WHAT IS CLAIMED IS:

1. A personal computer system comprising:

a core logic unit outputting first image data in a linear mode;

a graphics accelerator in communication with said core logic unit for processing said first image data into second image data in a linear mode;

a first tile converter in communication with said graphics accelerator for converting said second image data into third image data in a tile mode;

a local memory in communication with said first tile converter for storing therein said third image data;

a second tile converter in communication with said core logic unit for converting said first image data into fourth image data in a tile mode; and

a system memory accessible by said core logic unit, and comprising a graphics accelerating memory in communication with said second tile converter for storing therein said fourth image data.

2. The personal computer system according to claim 1 wherein said core logic unit includes a north bridge chip.

3. The personal computer system according to claim 1 wherein said graphics accelerator is a graphics chip.

4. The personal computer system according to claim 1 wherein said graphics accelerator, said first tile converter and said local memory are integrated into a graphics card.

5. The personal computer system according to claim 1 wherein said core logic unit, said graphics accelerator, said first tile converter and said second tile converter are integrated into a single core logic chip.

6. The personal computer system according to claim 1 wherein said local memory is disposed in said system memory.

7. The personal computer system according to claim 6 wherein said first tile converter and said second tile converter are integrated into a single tile converting device.

8. The personal computer system according to claim 1 wherein said graphics accelerating memory is an AGP (Accelerated Graphics Port) memory in communication with said core logic unit via an AGP protocol.

9. The personal computer system according to claim 1 further comprising a microprocessor in communication with said core logic unit.

10. A personal computer system comprising:

a core logic unit outputting first image data in a linear mode;

a graphics accelerator in communication with said core logic unit for processing said first image data into second image data in a linear mode;

a tile converting device having a first portion in communication with said graphics accelerator for converting said second image data into third image data in a tile mode and a second portion in communication with said core logic unit for converting said first image data into fourth image data in a tile mode;

a local memory in communication with said first portion of said tile converter for storing therein said third image data; and

a system memory accessible by said core logic unit, and comprising a graphics accelerating memory in communication with said second portion of said tile converter for storing therein said fourth image data.

11. The personal computer system according to claim 10 wherein said core logic unit includes a north bridge chip.

12. The personal computer system according to claim 10 wherein said graphics accelerator is a graphics chip.

13. The personal computer system according to claim 10 wherein said core

logic unit, said graphics accelerator and said tile converter are integrated into a single core logic chip.

14. The personal computer system according to claim 10 wherein said graphics accelerating memory is an AGP (Accelerated Graphics Port) memory in communication with said core logic unit via an AGP protocol.

15. The personal computer system according to claim 10 wherein said local memory is disposed in said system memory.

16. The personal computer system according to claim 10 further comprising a microprocessor in communication with said core logic unit.

17. A core logic chip for use in a personal computer system, said personal computer system comprising a system memory and a local memory, said core logic chip being integrated therein:

a core logic unit outputting first image data in a linear mode;

a graphics accelerator in communication with said core logic unit, processing said first image data into second image data in a linear mode;

a first tile converter in communication with said graphics accelerator, converting said second image data into third image data in a tile mode, and outputting said third image data to said local memory to be stored; and

a second tile converter in communication with said core logic unit, converting said first image data into fourth image data in a tile mode, and outputting said fourth image data to said system memory to be stored.

18. The core logic chip according to claim 17 wherein said first tile converter and said second tile converter are integrated into a single tile converting device.

19. The core logic chip according to claim 17 wherein said local memory is disposed in said system memory, and said third image data are stored in said local memory in said system memory.

20. The core logic chip according to claim 17 wherein said fourth image data is stored in an AGP (Accelerated Graphics Port) memory disposed in said system memory.